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69	4	(integrated adj circuit \$5processor \$5controller) near3 loop same hardware same model\$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:27
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98	23	(integrated adj circuit \$5processor \$5controller) near5 loop and hardware same (model\$ simulat\$ emulat\$) and (@ad<19990813 @rlad<19990813) and @pd>20040218	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/07/27 18:53



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1 High quality desktop video conferencing using agent based systems

Catrava, S.;

Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on , 27-29 March 1996

Pages:37 - 43

[\[Abstract\]](#) [\[PDF Full-Text \(588 KB\)\]](#) **IEEE CNF**

2 Architectural and compiler support for energy reduction in the memory hierarchy of high performance microprocessors

Hajj, N.B.M.; Polychronopoulos, C.; Stamoulist, G.;

Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on , 10-12 Aug. 1998

Pages:70 - 75

[\[Abstract\]](#) [\[PDF Full-Text \(524 KB\)\]](#) **IEEE CNF**

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Supercomputing '94. Proceedings, 14-18 Nov. 1994

Pages:488 - 497

[\[Abstract\]](#) [\[PDF Full-Text \(764 KB\)\]](#) **IEEE CNF****2 Effective hardware-based data prefetching for high-performance processors***Tien-Fu Chen; Jean-Loup Baer;*

Computers, IEEE Transactions on, Volume: 44, Issue: 5, May 1995

Pages:609 - 623

[\[Abstract\]](#) [\[PDF Full-Text \(1408 KB\)\]](#) **IEEE JNL****3 A loop partition technique for reducing cache bank conflict in multithreaded architecture***Wu, C.-C.; Chen, C.F.;*

Computers and Digital Techniques, IEE Proceedings-, Volume: 143, Issue:

1, Jan. 1996

Pages:30 - 36

[\[Abstract\]](#) [\[PDF Full-Text \(718 KB\)\]](#) **IEEE JNL****4 Compiler algorithms for optimizing locality and parallelism on shared and distributed memory machines***Kandemir, M.; Ramanujam, J.; Choudhary, A.;*

Parallel Architectures and Compilation Techniques., 1997. Proceedings. 1997

International Conference on, 10-14 Nov. 1997

Pages:236 - 247

[\[Abstract\]](#) [\[PDF Full-Text \(1116 KB\)\]](#) **IEEE CNF**

5 Architectural and compiler support for energy reduction in the memory hierarchy of high performance microprocessors

Hajj, N.B.M.; Polykronopoulos, C.; Stamoulis, G.;

Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on , 10-12 Aug. 1998

Pages:70 - 75

[\[Abstract\]](#) [\[PDF Full-Text \(524 KB\)\]](#) [IEEE CNF](#)

6 Bounds-based loop performance analysis: application to validation and tuning

Bose, P.; Kim, S.; O'Connell, F.P.; Ciarfella, W.A.;

Performance, Computing and Communications, 1998. IPCCC '98., IEEE International , 16-18 Feb. 1998

Pages:178 - 184

[\[Abstract\]](#) [\[PDF Full-Text \(596 KB\)\]](#) [IEEE CNF](#)

7 Software versus hardware coherence: performance versus cost

Zucker, R.N.; Baer, J.-L.;

System Sciences, 1994. Vol. I: Architecture, Proceedings of the Twenty-Seventh Hawaii International Conference on , Volume: 1 , 4-7 Jan. 1994

Pages:163 - 172

[\[Abstract\]](#) [\[PDF Full-Text \(648 KB\)\]](#) [IEEE CNF](#)

8 A three-million-transistor microprocessor

Abu-Nofal, F.; Avra, R.; Bhabuthmal, K.; Bhamidipaty, R.; Blanck, G.; Charnas, A.; DelVecchio, P.; Grass, J.; Grinberg, J.; Hayes, N.; Haber, G.; Hunt, J.; Kizhepat, G.; Malamy, A.; Marston, A.; Mehta, K.; Nanda, S.; Van Nguyen, H.; Patel, R.; Ray, A.; Reaves, J.; Rogers, A.; Rusu, S.; Shay, T.; Sidharta, I.; Tham, T.; Tong, P.; Trauben, R.; Wong, A.; Yee, D.; Maan, N.; Steiss, D.; Youngs, L.;

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Pages:108 - 109, 257

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) [IEEE CNF](#)

09637984_QUAL

5768567	66
6212489	66
6212489	66
6230114	57
5911059	57
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6751583	57
6026230	57
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5678028	57
5353243	57
5625580	57
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6321366	57
6389379	57
6421251	57
5740183	55
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5881267	50
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6016554	49
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6393569	49
6466996	49
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5758123	48

09637984_QUAL

5991533 48
5991529 48
